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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,363	11/20/2003	Jiaw-Ren Shih	TS01-1493	9515

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,363	SHIH ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *21-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/18/2004 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 1-20 in the Paper filed 10/18/2004 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 11/20/2003 is acceptable.

Drawings

4. The formal drawings filed on 11/20/2003 are acceptable.

Priority

5. Applicants have made no claim for priority.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 01/29/2004 has been considered.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

8. Claims 1,7,8,9,10,11,12,13,15,22,23, and 24 are objected to because of the following informalities:

A. There is no apparent antecedent basis for "another said pair," "said protection structure," or "said n-th pair" in claim 1.

B. There is no apparent antecedent basis for "said first doped N-Well region," in claim 7.

C. There is no apparent antecedent basis for "the collector," "said first PNP," "the base," "said first parasitic NPN," or "the anode" in claim 8.

D. There is no apparent antecedent basis for "said third doped N+ region," "the cathode," "said second diode," "the emitter," or "said first parasitic NPN," in claim 9.

E. There is no apparent antecedent basis for "said second doped P+ region," "the anode," or "the emitter," in claim 10.

F. There is no apparent antecedent basis for "the cathode," "said first doped N-Well region," "said third diode," "the base," or "said second parasitic PNP" in claim 11.

G. There is no apparent antecedent basis for "the collector," "said second PNP parasitic," "said second parasitic bipolar NPN," or "the anode" in claim 12.

H. There is no apparent antecedent basis for "said third doped N+ region," "the cathode," "said fourth diode," "the emitter," or "said second NPN" in claim 13.

I. There is no apparent antecedent basis for "said third doped N+ region," "said second doped pair," "the n-1 conductor," "the n-1 doped pair," or "the nth doped pair" in claim 15.

J. There is no apparent antecedent basis for "said first doped N-Well region," in claim 22.

K. There is no apparent antecedent basis for "the collector," "said PNP," "the base," "said parasitic NPN," or "the anode" in claim 23.

L. There is no apparent antecedent basis for "the cathode," "said second diode," "the emitter," or "said parasitic NPN," in claim 24.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 16 and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by LEE ET AL. (6,249,414).

Lee et al. discloses a power-to-power semiconductor ESD protection structure with a first dopant type (p-type) semiconductor substrate 11, an opposite dopant type (n-type) first doped region 23 within said substrate 11; a first dopant type (p-type) second doped region 14 within said first doped region 23; an opposite dopant type (n-type) third doped region 16 within said substrate 11 which when taken with said second doped region 14 forms a doped pair, a conductor element from said second doped region 14 to a first voltage source 19; and a conductor element from said third doped region 16 to a second voltage source 20, wherein said second doped region 14 is an anode of a first diode protection structure and an emitter of a parasitic bipolar PNP transistor, said first doped region 23 is a cathode of the first diode protection element and also a base of the parasitic bipolar PNP transistor and a collector of a parasitic bipolar NPN transistor, said substrate 11 is a collector of the parasitic bipolar PNP transistor, a base of the parasitic bipolar NPN transistor, and an anode of a second diode protection element, and said third doped region 16 is a cathode of the second diode protection element and an emitter of the parasitic bipolar NPN transistor. Note figures 3 and 4 of Lee et al.

B. Claims 1 and 6-15 rejected under 35 U.S.C. 102(b) as being anticipated by LEE ET AL. (6,271,999).

Lee et al. discloses a power-to-power semiconductor ESD protection structure with a first dopant (p) type semiconductor substrate 300, opposite (n) dopant type multiple first doped regions 305a, 305c, 305e, etc. (note that doped regions 305b, 305d, 305f,

etc, along with regions 310b, 310d, 310f, etc., form the claimed multiple third doped regions 305-310b, 305-310d, 305-310f) within said substrate 300; first dopant (p) type multiple second doped regions 315a, 315c, 315e, etc., one of each of said multiple second doped regions 315a, 315c, 315e, etc. within each of said multiple first doped regions 305a, 305c, 305e, etc.; opposite (n) dopant type multiple third doped regions 305-310b, 305-310d, 305-310f within said substrate 300, each of which together with one of said multiple second doped regions 315a, 315c, 315e, etc., forms a doped pair, multiple conductor elements 360 each one connecting one said third doped region of one said doped pair to one said second doped region of another said pair (for example, the first of the third doped regions, element 305-310b, is connected to a second doped element of a second doped pair, said second doped element not shown, but nominally 315c) starting with a third doped region 305-310b of a first doped pair 305-310b-315a and ending with a second doped region (not shown, nominally 315ℓ, the third doped region of the nth pair being 305-310m) of an nth doped pair 305-310m-315ℓ, to form an electrical series string of protection structure element pairs; a conductor element 320 from a second doped element 315a of said first doped pair 305-310b-315a to a first voltage source V1; and a conductor element 325 from a third doped element 310m of said nth doped pair 305-310m-315ℓ to a second voltage source V2, wherein a second doped region 315a of the first doped pair 305-310b-315a is an anode of a first diode protection element and an emitter of a first parasitic bipolar PNP transistor, a first doped region 305a associated with said first doped pair 305-310b-

315a is a cathode of said first diode protection element and also a base of said first parasitic bipolar PNP transistor and a collector of a first parasitic bipolar NPN transistor, said substrate 300 is a collector of said first parasitic bipolar PNP transistor, a base of said first parasitic bipolar NPN transistor, and an anode of a second diode protection element, said third doped region 305-310b of said first doped pair 305-310b-315a is a cathode of said second diode protection element and an emitter of said first parasitic bipolar NPN transistor, a second doped region 315c of a second doped pair 305-310d-315c is an anode of a third diode protection structure and an emitter of a second parasitic bipolar PNP transistor, a first doped region 305c which contains said second doped region 315c of said second doped pair 305-310d-315c is a cathode of said third diode protection device structure and a base of said second parasitic bipolar PNP transistor, said substrate 300 is the collector of said second parasitic bipolar PNP transistor, the base of a second parasitic bipolar NPN transistor, and the anode of a fourth diode protection device structure, a third doped region 305-310d of said second doped pair 305-310d-315c is a cathode of said fourth diode protection device, and an emitter of said second parasitic bipolar NPN transistor, and wherein the protection structure element pairs are repeated for n doped pairs, whereby n is nominally 6, thus between two to ten, and a first conductor element of said multiple conductor elements 360 connects said third doped region 305-310b of said first doped pair 305-310b-315a to said second doped region 315c of said second doped pair 305-310d-315c and an n-1 conductor element of said multiple conductor

elements 360 connects a third doped region 305-310k of an n-1 doped pair 305-310k-315j with said second doped region 315ℓ of said nth doped pair 305-310m-315ℓ. Note figures 3 and 4 of Lee et al.

C. Claims 16,17, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by WATANABE (3,806,773).

Watanabe discloses a power-to-power semiconductor ESD protection structure with a first dopant type semiconductor substrate 1, P doped with a concentration between 1E15 and 5E15 a/cm3; an opposite dopant type first doped region 3, doped with a donor dopant to form a N-well region with a typical dopant density of 1E18 a/cm3, which is between 1E16 and 1E18 a/cm3, within said substrate 1; a first dopant type second doped region 4 within said first doped region 3; an opposite dopant type third doped region 6d, doped with a donor dopant to form an N+ region with a dopant concentration of between 1E20 and 1E21 a/cm3, within said substrate 1 which when taken with said second doped region 4 forms a doped pair 4-6d, a conductor element 8d from said second doped region 4 to a first voltage source D; and a conductor element 9a from said third doped region 6d to a second voltage source G. Note figure 2 and column 2 lines 40-60 of Watanabe.

D. Claims 16,18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by ITO (5,604,655).

Ito discloses a power-to-power semiconductor ESD protection structure with a first dopant type (p-type) semiconductor substrate 13, an opposite dopant type (n-type)

first doped region 14 doped with a donor dopant to form a N-well region with a typical dopant density of 10^{18}/cc, which is between 1E16 and 1E 18 a/cm3, within said substrate 13; a first dopant type (p-type) second doped region 20 doped with an acceptor dopant to form P+ regions with a dopant concentration of 10^{20}/cc, which is between 1E20 and 1E21 a/cm3, within said first doped region 14; an opposite dopant type (n-type) third doped region 36 within said substrate 13 which when taken with said second doped region 20 forms a doped pair 20-36, a conductor element 23a from said second doped region 20 to a first voltage source (input voltage "i"); and a conductor element 23d from said third doped region 36 to a second voltage source (ground). Note figures 6-9, column 6 line 60, and column 7 line 10 of Ito.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over LEE ET AL. (6,271,999) in view of BORLAND (5,814,866).

Lee et al. discloses a power-to-power semiconductor ESD protection structure with all the limitations of claims 2 and 3 except that the substrate be doped p-type at a

concentration of 1-5 times 10^{15}/cc and that the first doped region (well region) be doped n-type at a concentration of 10^{16}/cc - 10^{18}/cc. Note figures 3 and 4 of Lee et al.

However, Borland discloses a semiconductor ESD protection structure with a substrate doped p-type at a concentration of 1-5 times 10^{15}/cc and a first doped region (well region) doped n-type at a concentration of .1-10 times 10^{17}/cc. Note claim 9 of Borland. Therefore, it would have been obvious to a person having skill in the art to replace the substrate and first doped regions of Lee et al.'s power-to-power semiconductor ESD protection structure with the substrate doped p-type at a concentration of 1-5 times 10^{15}/cc and the first doped region (well region) doped n-type at a concentration of .1-10 times 10^{17}/cc such as taught by Borland in order to increase substrate resistance and to form a clear-cut PN junction between well and substrate to thus provide a better substrate-well junction and minimize substrate leakage.

B. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over LEE ET AL. (6,271,999) in view of CURRY ET AL. (5,761,697).

Lee et al. discloses a power-to-power semiconductor ESD protection structure with all the limitations of claims 4 and 5 except that the second doped regions be doped with an acceptor dopant to form P+ regions with a dopant concentration between 1E20 and 1E21 a/cm3, and that the third doped regions be doped with a donor dopant to form N+ region(s) with a dopant concentration of between 1E20 and 1E21 a/cm3. Note figures 3 and 4 of Lee et al.

However, Curry et al. discloses a semiconductor ESD protection structure with second doped regions 121A doped with an acceptor dopant to form P+ regions with a dopant concentration between 1E20 and 1E21 a/cm3, and third doped regions 151 doped with a donor dopant to form N+ region(s) with a dopant concentration of between 1E20 and 1E21 a/cm3. Note figures 16K and 16N, and column 23 lines 48-50 and 60-64 of Curry et al. Therefore, it would have been obvious to a person having skill in the art to replace the second and third doped regions of Lee et al.'s power-to-power semiconductor ESD protection structure with the second doped regions doped with an acceptor dopant to form P+ regions with a dopant concentration between 1E20 and 1E21 a/cm3, and third doped regions doped with a donor dopant to form N+ region(s) with a dopant concentration of between 1E20 and 1E21 a/cm3, such as taught by Curry et al., in order to provide ohmic contact to the wirings attached to these two regions to thus provide a better discharge path.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
12/04